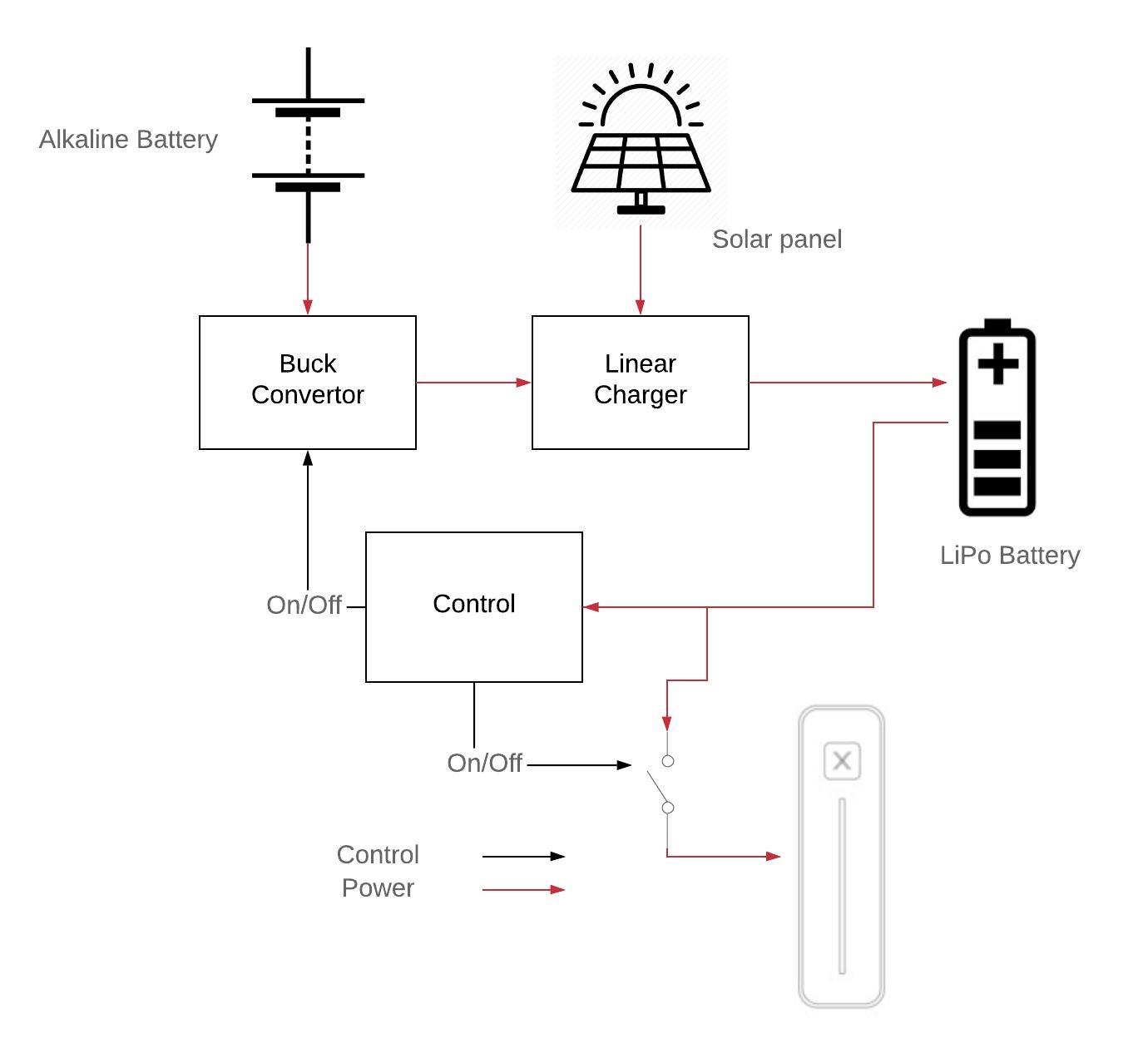
New Charger design for Gear I

# The problem to be addressed

# Top Diagram



# Description

## The Alkaline AA battery array

The array is consist of 12 AA batteries. The capacity of each battery is between [500mAh@500mA](mailto:500mAh@500mA) and [1100mAh@25mA](mailto:1100mAh@25mA). The alkaline power is from 8V to 18V.

## The solar panel

## The buck converter

The buck converter step down alkaline power to 9Vdc. The efficiency is expected to be above [90%@100mA](mailto:90%25@100mA), [80%@10mA](mailto:80%25@10mA) and [50%@1mA](mailto:50%25@1mA).

The buck is enabled when ***Vbatt***<7.75V, and disabled when ***Vbatt***>7.85V.

The ripple voltage is expected to be below 100mV.

The quiescent current when the buck is disabled is expected to be below 20uA.

## The linear charger

The linear charger is powered by either 9Vdc from the buck or solar panel.

The linear charger is always on.

The quiescent current when the linear charger is not powered up is expected to be below 10uA.

The linear charger should stop charging when ***Vbatt***>8.2V, and restart charging when ***Vbatt***<8.1V.

The linear charger should start trickle charging when ***Vbatt***<6.0V, and restart normal charging when ***Vbatt***>6.2V.

## The charging control

The charging control circuitry is designed to output ***EN\_BUCK*** and ***EN\_LOAD***. The ***EN\_BUCK*** turn ON/OFF the buck converter. The ***EN\_LOAD*** turn ON/OFF the system.

The schmitt window of ***EN\_BUCK*** is from 7.75V to 7.85V.

The schmitt window of ***EN\_LOAD*** is from 6.0V to 6.5V.

## The LiPo battery

The LiPo battery pack is consist of 2 cells of lithium-polymer in serial, with over-charging, under-charging, thermal protection and cell-balancing.

The capacity of the LiPo pack is ???.

# Buck converter of Alkaline power

Reference to datasheet of TPS54061 & ‘052350-9R Axis Apollo Calculation.ods’

## Enable glitch filter

In order to remove the glitch on ***EN\_BUCK,*** a low pass filter is implemented. Due to the internal pull-up resistance(around 5MOhm) on EN pin. The serial resistance of the low pass filter can not be larger than 200k. Otherwise, the buck will never be turned off.

# Linear charger

Reference to datasheet of TPS54061 & ‘052350-9R Axis Apollo Calculation.ods’

## Pull up resistor of CC pin

Value of pull-up resistor of CC pin should be as large as possible to reduce the quiescent current.

## Value of Rt1 & Rt2

Value of Rt1 & Rt2 should be as large as possible to reduce the quiescent current.

# Control circuit

## Voltage Reference:

The 3.3V reference is generated by a shunt diode(D1), the minimum working current is 1uA. Then divide 3.3V to 1.65V reference by two resistors.

The shunt reference only sources current. In order to sink current, a follower(OP1) buffers the reference and output Vref1.65V.

Vref1.65V is used as bias for non-inverting Schmitt comparator(OP2) and inverting Schmitt comparator(OP3).

The shunt diode(D1) is working at 1.5uA. Current of R2 & R3 is set to 1uA.

## Vbatt sensing divider:

When, R6 & R7 divided Vbatt to 1.65V. The divided Vbatt is buffered by OP4 and then feed into non-inverting Schmitt comparator(OP2) later.

The input resistance of non-inverting Schmitt comparator(OP2) paralleled by R7 may change the divider, so the follower(OP4) is implemented.

When , R4 & R5 divided Vbatt to 1.65V. The divided Vbatt is feed into inverting Schmitt comparator(OP3) later.

Current of R4 & R6 are all set to 1uA.

## Lower threshold (6V-6.5V) non-inverting Schmitt comparator:

OP2 is a non-inverting Schmitt comparator. Set Vss of OP3 0V. Set Vcc of OP3 3.3V.

The Schmitt window is calculated as:

The corresponding Vbatt of the Schmitt window is 6V~6.5V

OP2 must have a very low input bias current**(<1pA)**, so that the bias current doesn’t affect the divider.

OP2 must be a **Rail-to-Rail** output.

The current per channel of OP2 should be low**(<1uA)**

In order to fully close a PFET, the ‘Vg’ should be adapted to 0-Vbatt range by a N-FET.

## Higher threshold (7.75-7.85V) Schmitt comparator:

OP3 is an inverting Schmitt comparator. Set Vss of OP3 0V. Set Vcc of OP3 3.3V.

The Schmitt window is calculated as:

The corresponding Vbatt of the Schmitt window is 7.75V~7.85V

OP3 must have a very low input bias current**(<1pA)**, so that the bias current doesn’t affect the divider.

The current per channel of OP2 should be low**(<1uA)**

OP3 must be a **Rail-to-Rail** output.

## 3.3V LDO:

Vbatt is regulated to 3.3V for OP-amps. The LDO should have low quiescent current**(<2uA)**.

## Cost estimate (option1)

TLV8544 \*1: $0.3 \*1

ZXRE330ASA \*1: $0.3 \*1

NCP551SN50T1G \*1: $0.2 \*1

NMOS\*1: $0.1 \*1

## Current estimate:

Op-amp 0.5uA \*4 = 2.0uA

Shunt diode 1.5uA

Divider resistors 1uA\*3 = 3uA

LDO Iq 1uA max

R8 & R9 1uA max

R10 & R11 1uA max

Ids of M1 1uA